

FIG. 1A

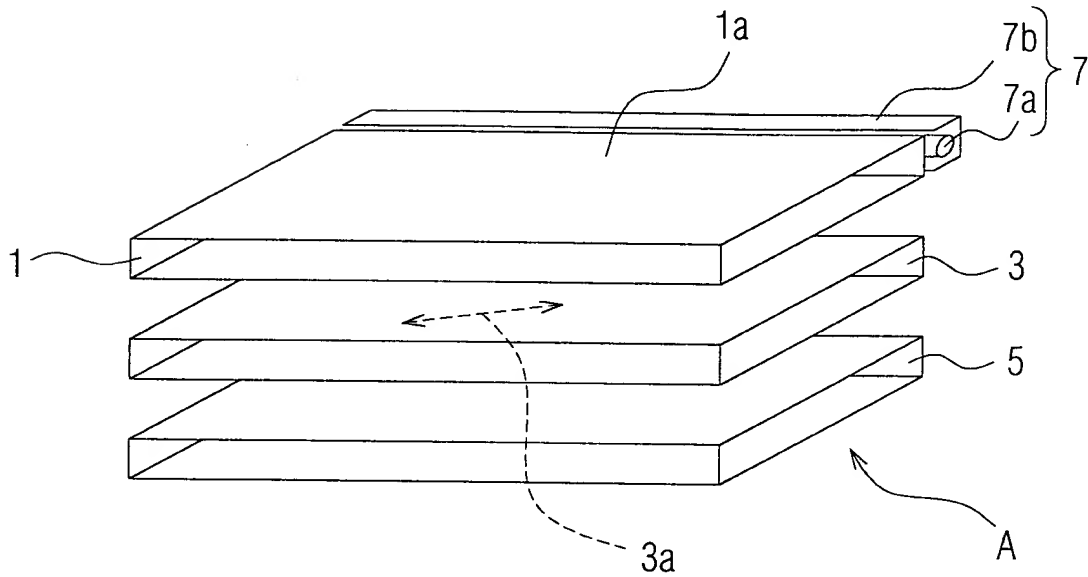


FIG. 1B

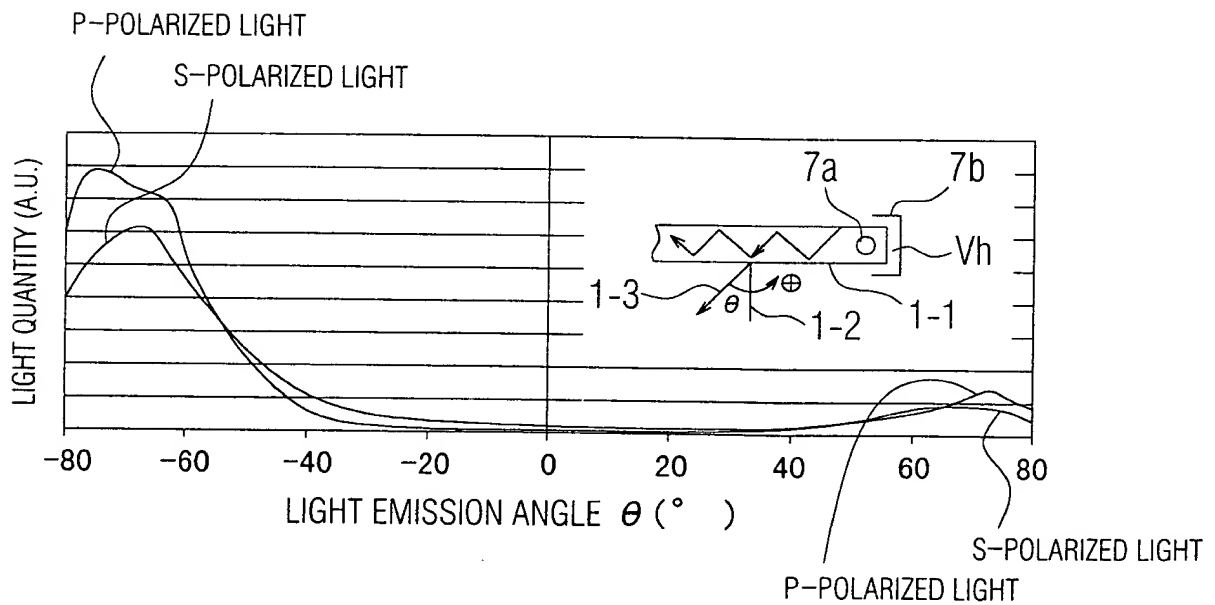


FIG. 2 A

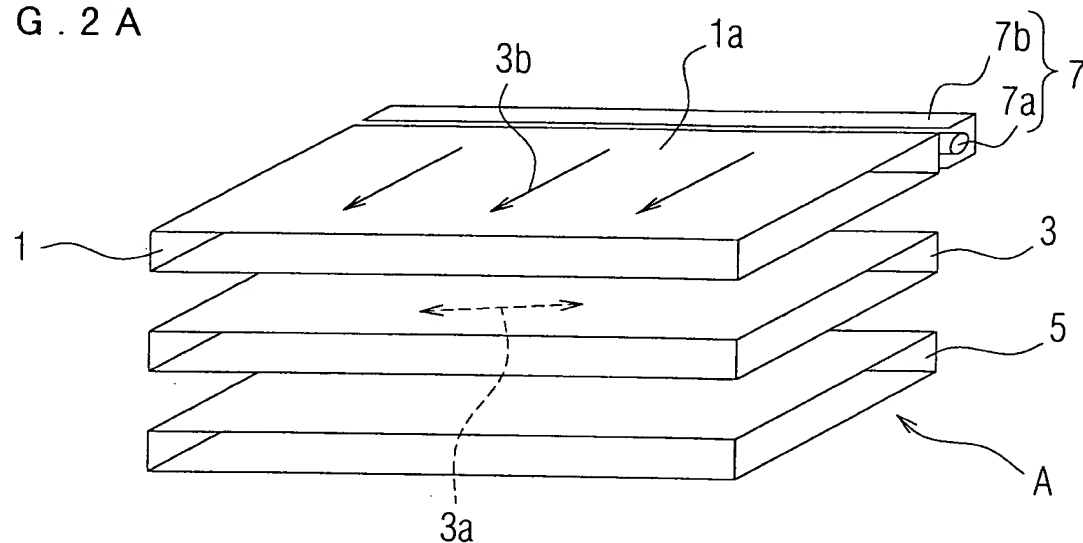


FIG. 2 B

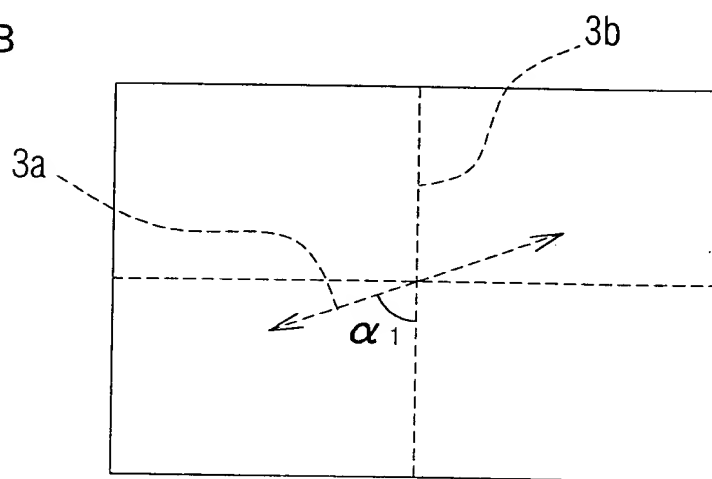
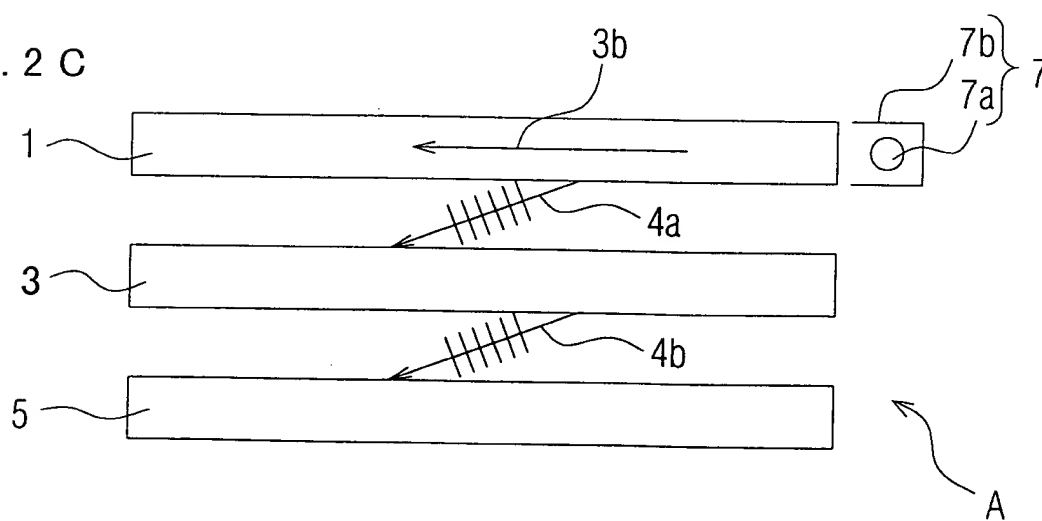


FIG. 2 C



This diagram illustrates a cross-sectional view of a semiconductor device along a plane E-E. The device consists of a substrate 101 with a patterned layer 103 and a top layer 105. A central region 110 is defined by a dashed line E-E. The left side shows a cross-section of a wafer 3 and a stack of layers 152, 154, and 128b. The right side shows a more complex structure with layers 128a, 146, and 144.

FIG. 4 A

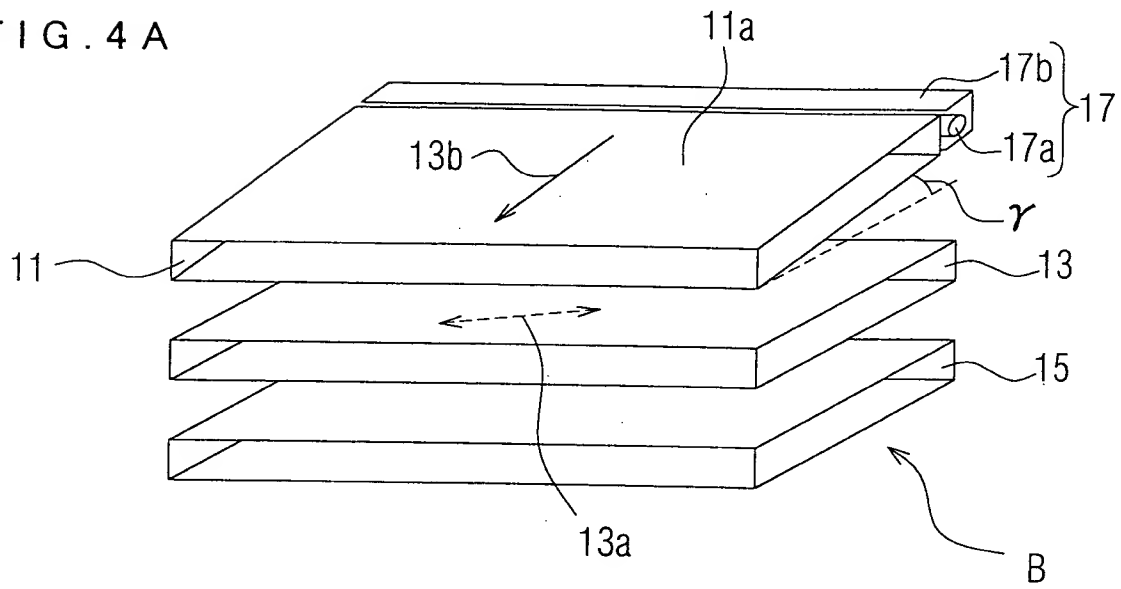


FIG. 4 B

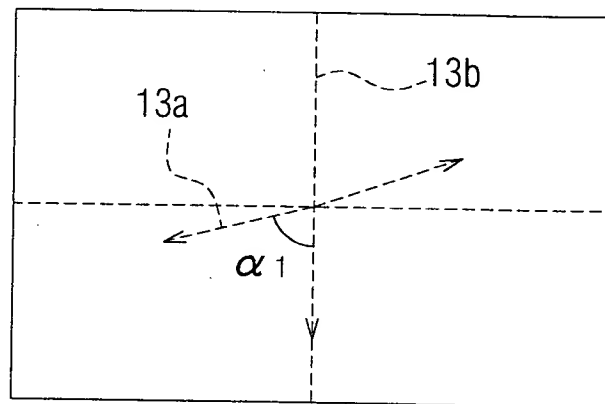


FIG. 4 C

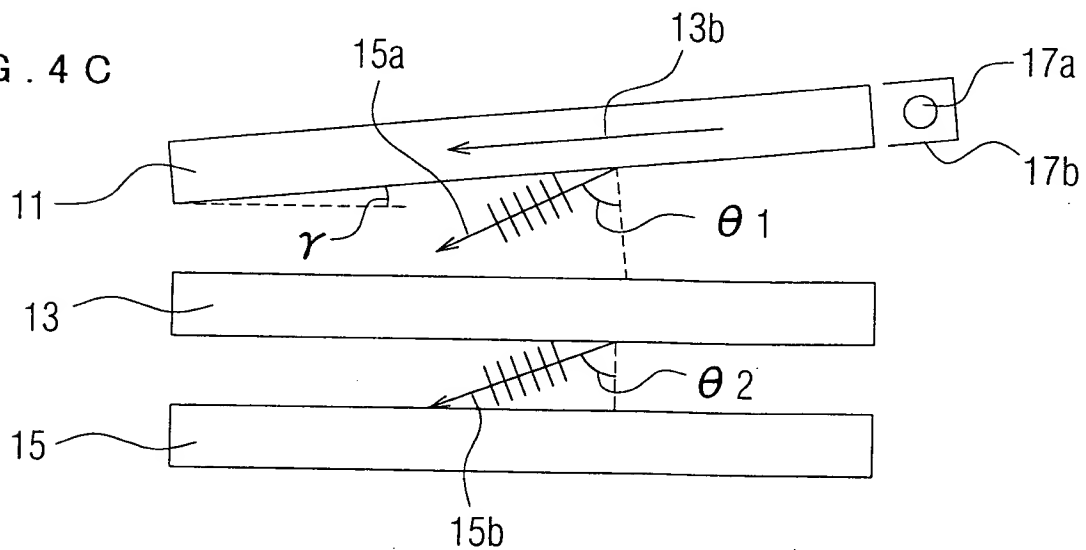
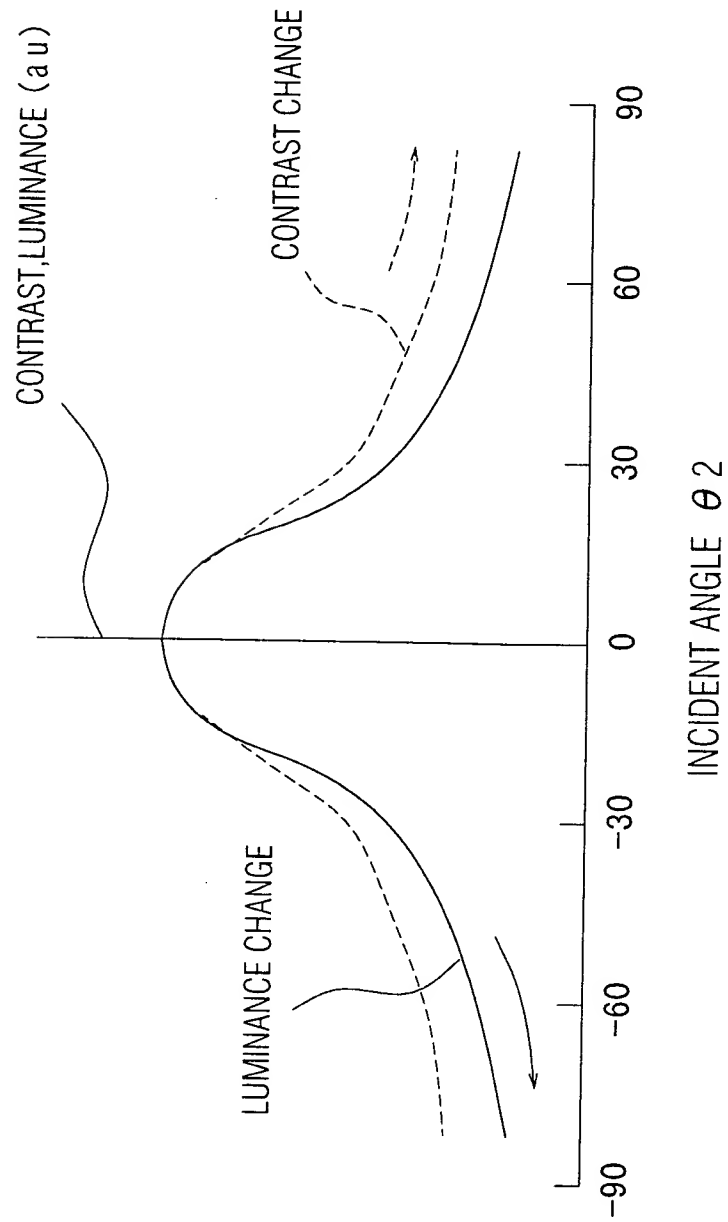


FIG. 5



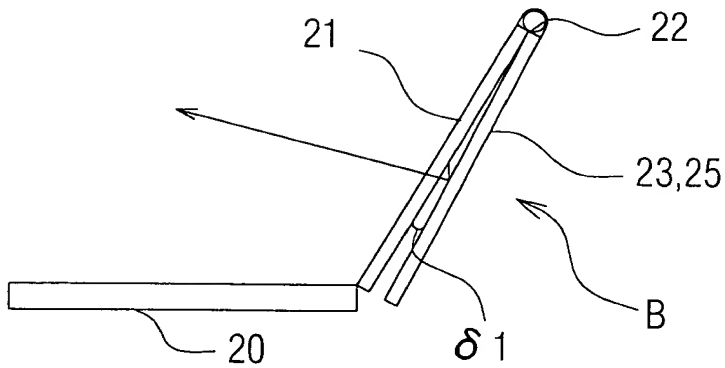


FIG. 6 A

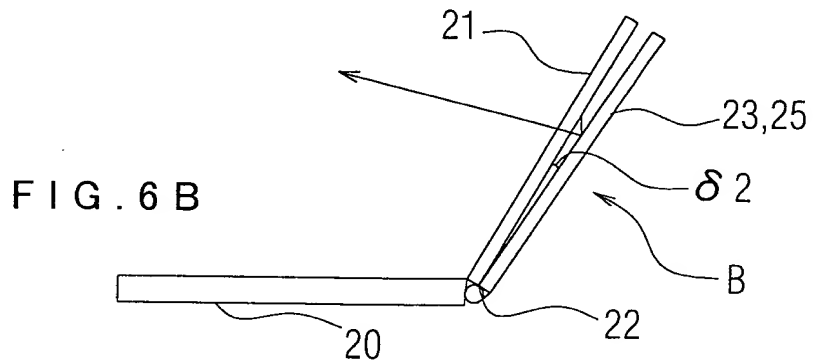


FIG. 6 B

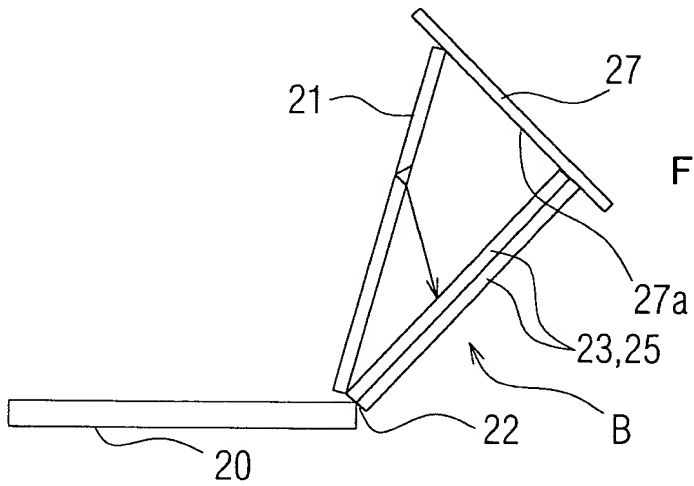


FIG. 6 C

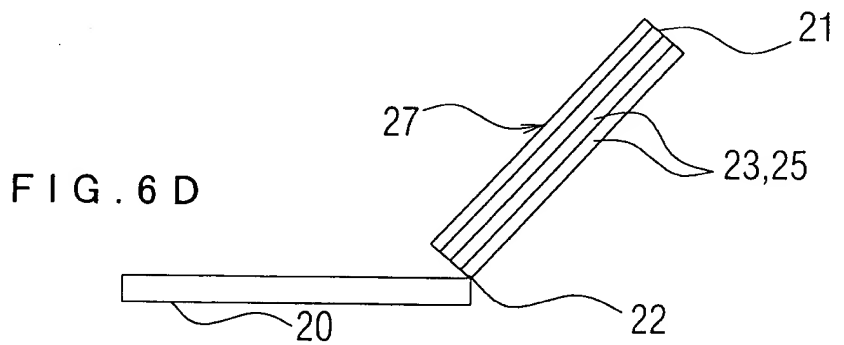


FIG. 6 D

FIG. 6 E

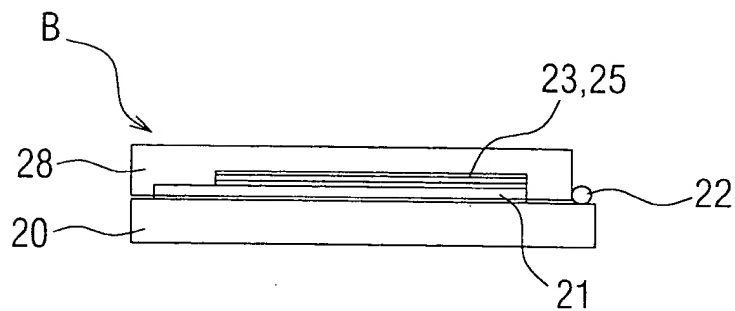


FIG. 6 F

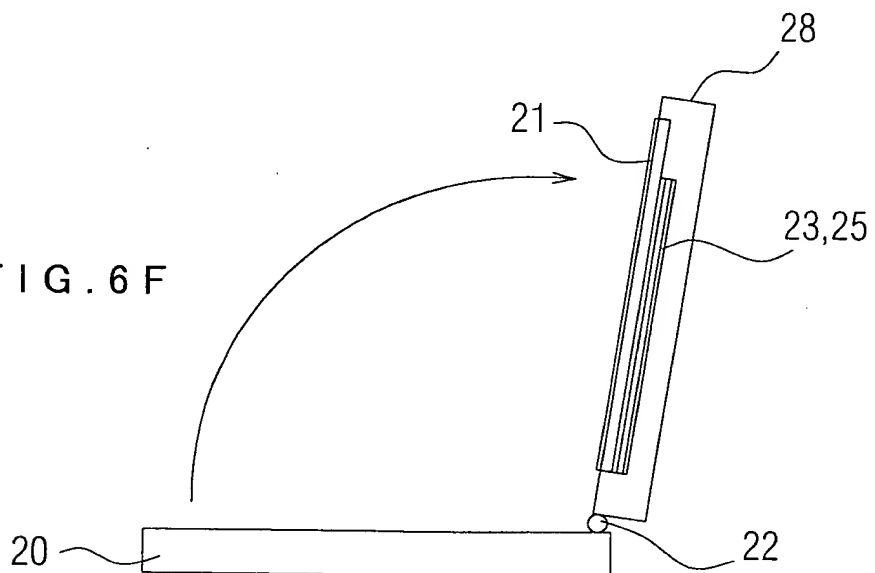


FIG. 6 G

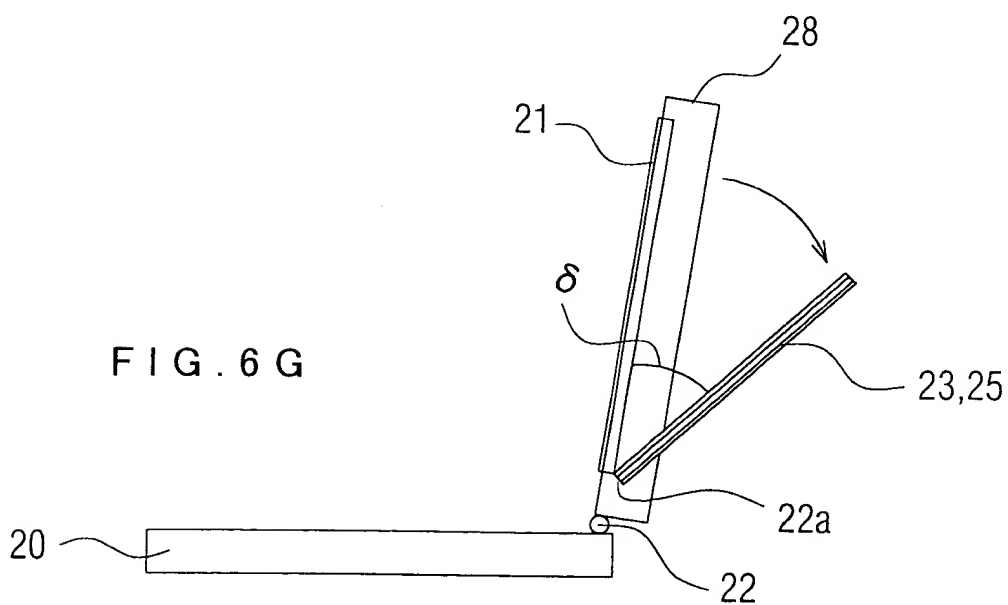


FIG. 7 A

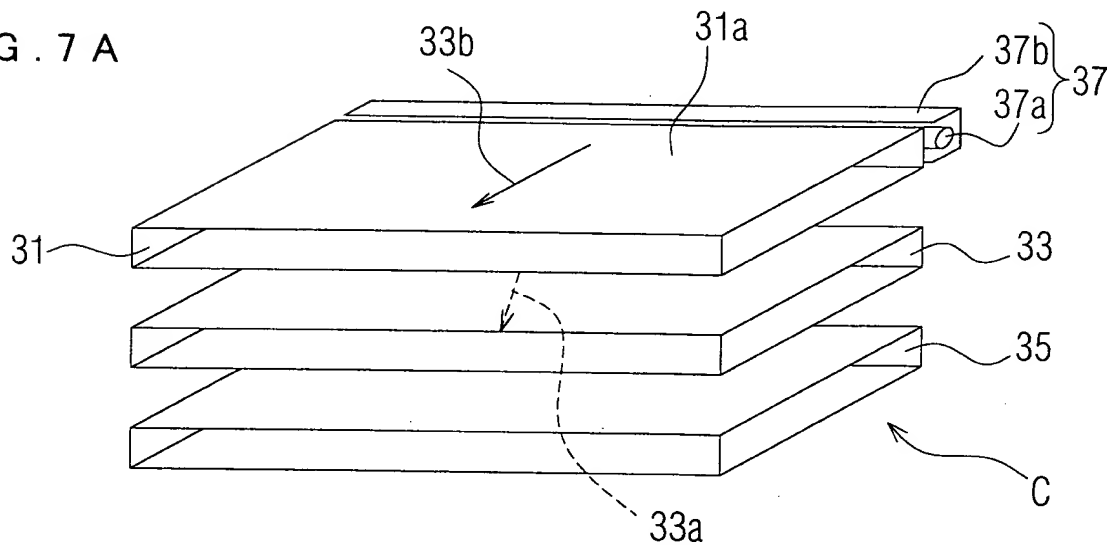


FIG. 7 B

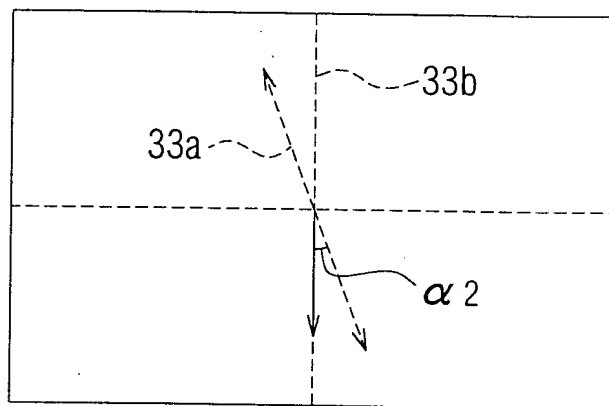


FIG. 7 C

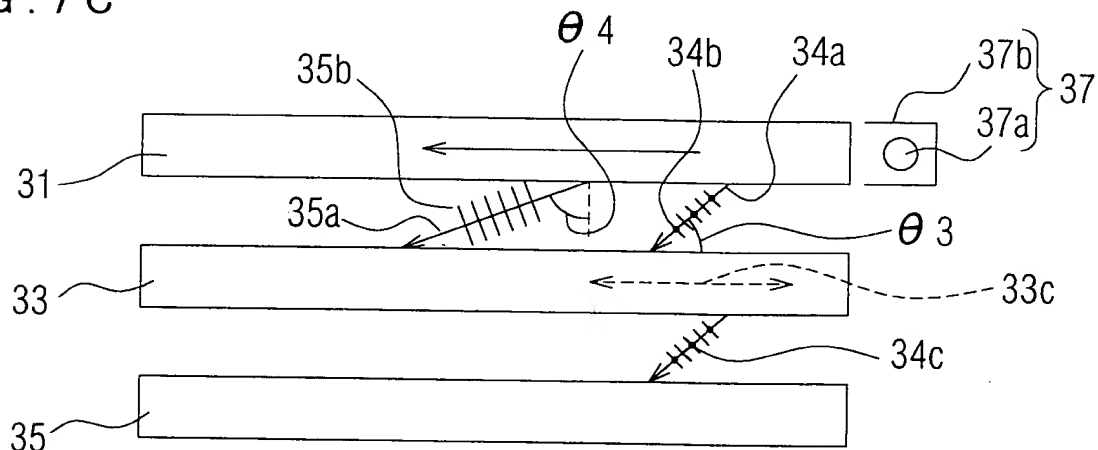




FIG. 8 A

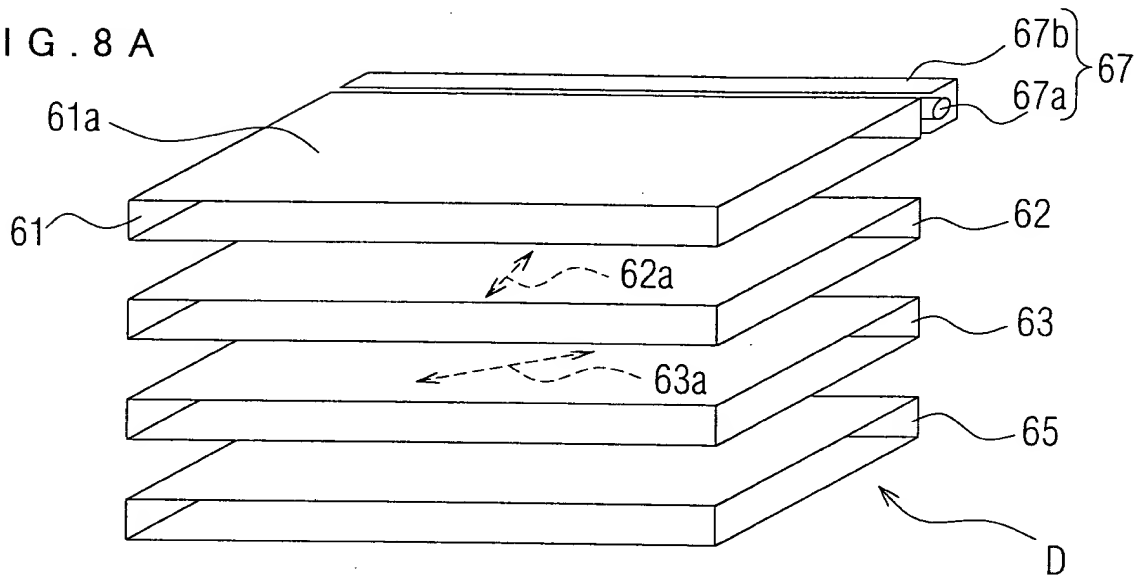


FIG. 8 B

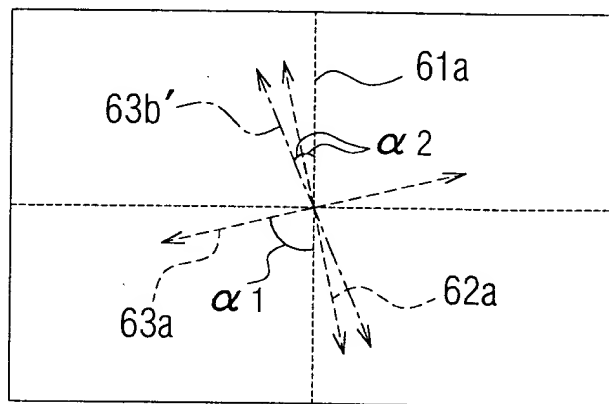


FIG. 8 C

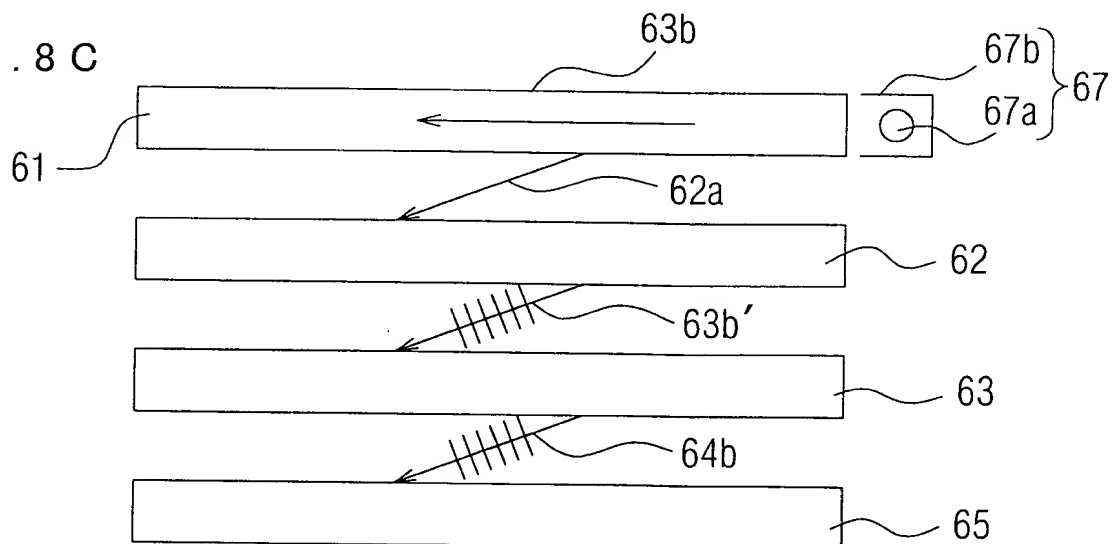
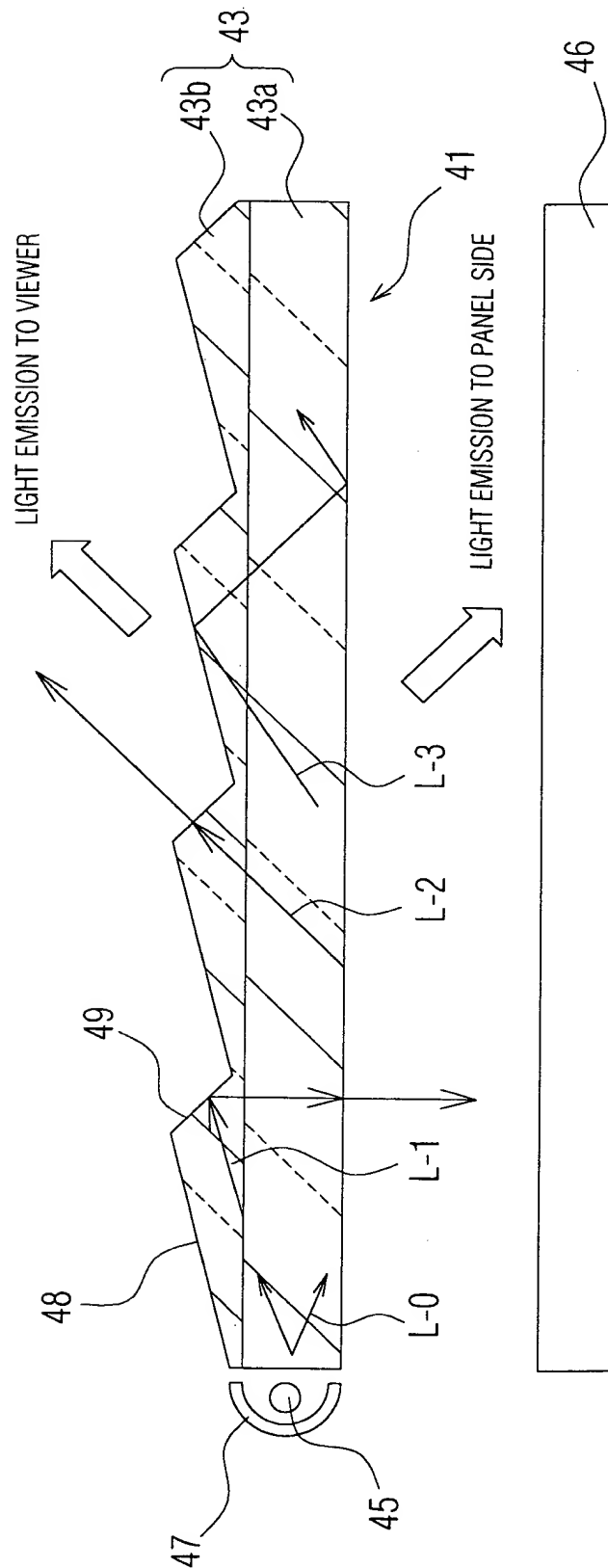


FIG. 9





[illegible]

FIG. 12

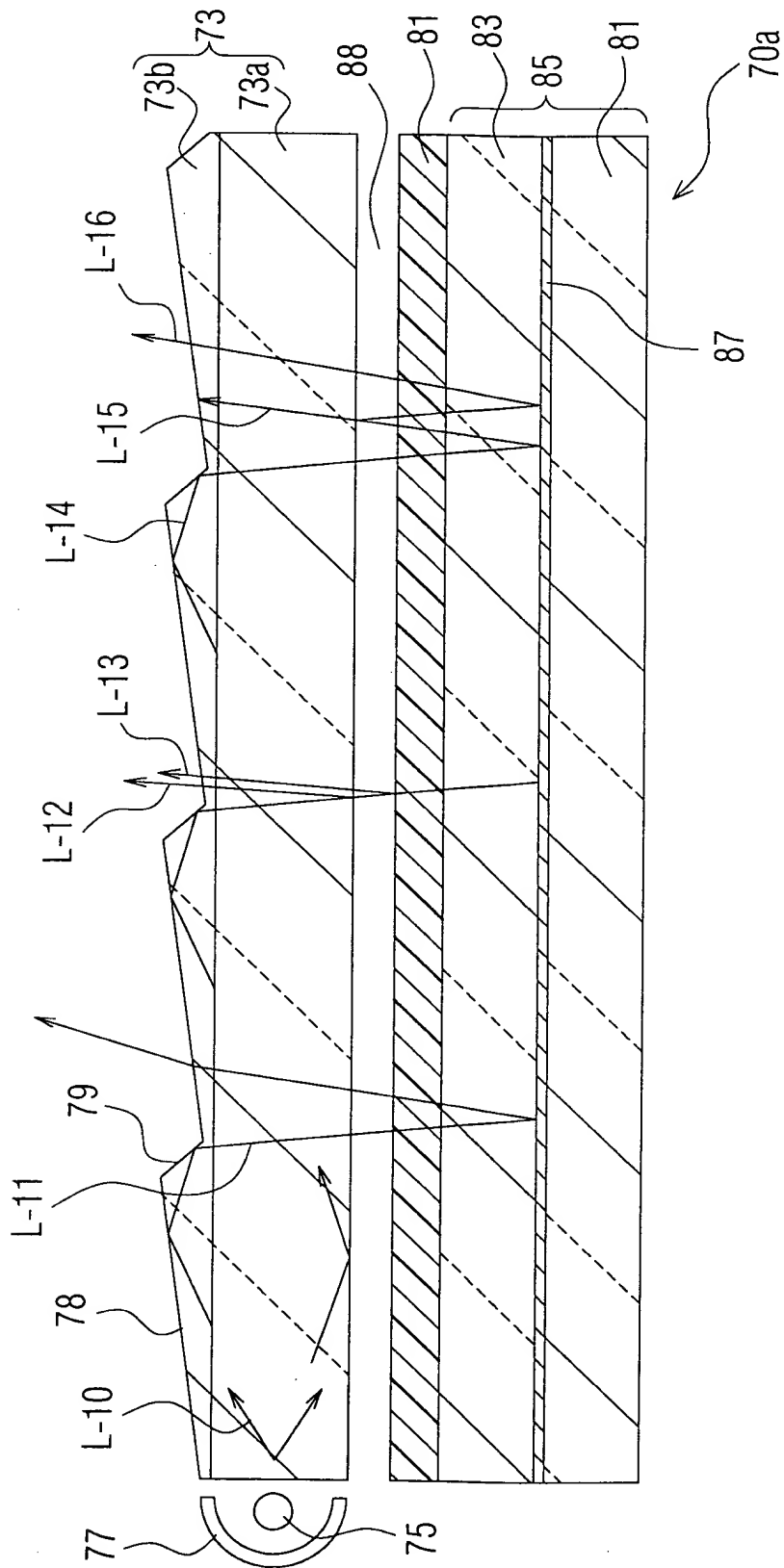


FIG. 13

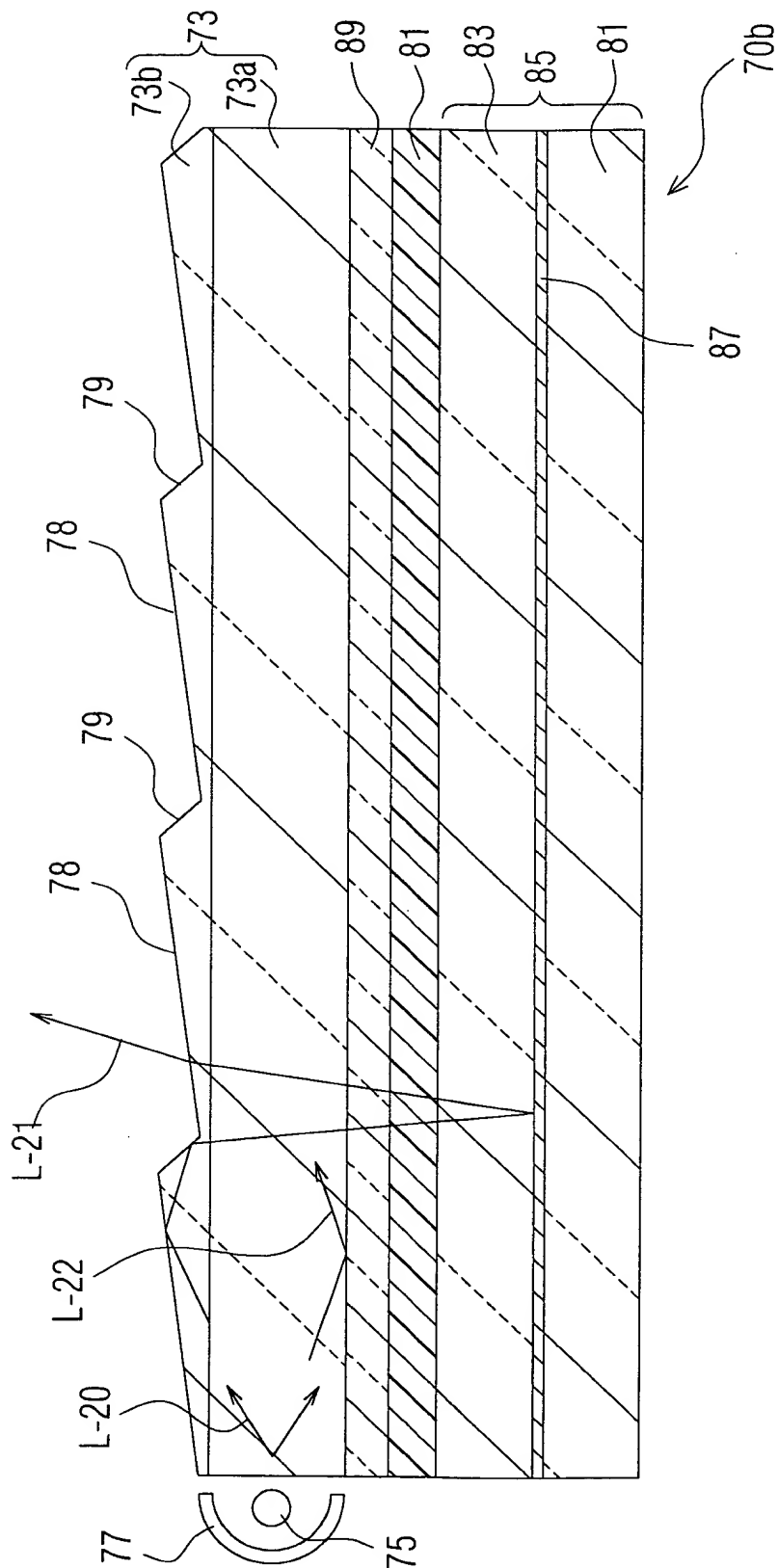


FIG. 14

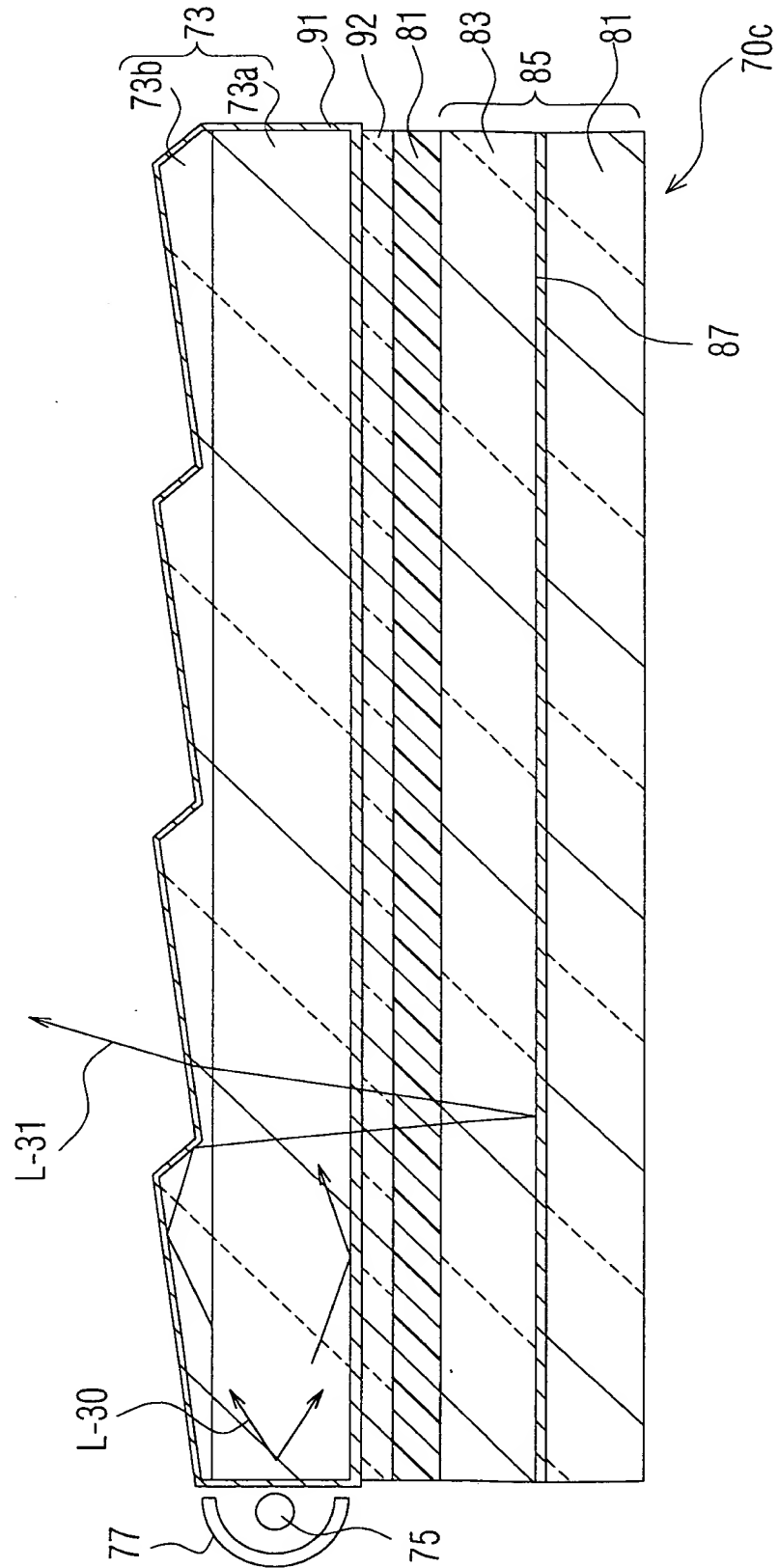


FIG. 15

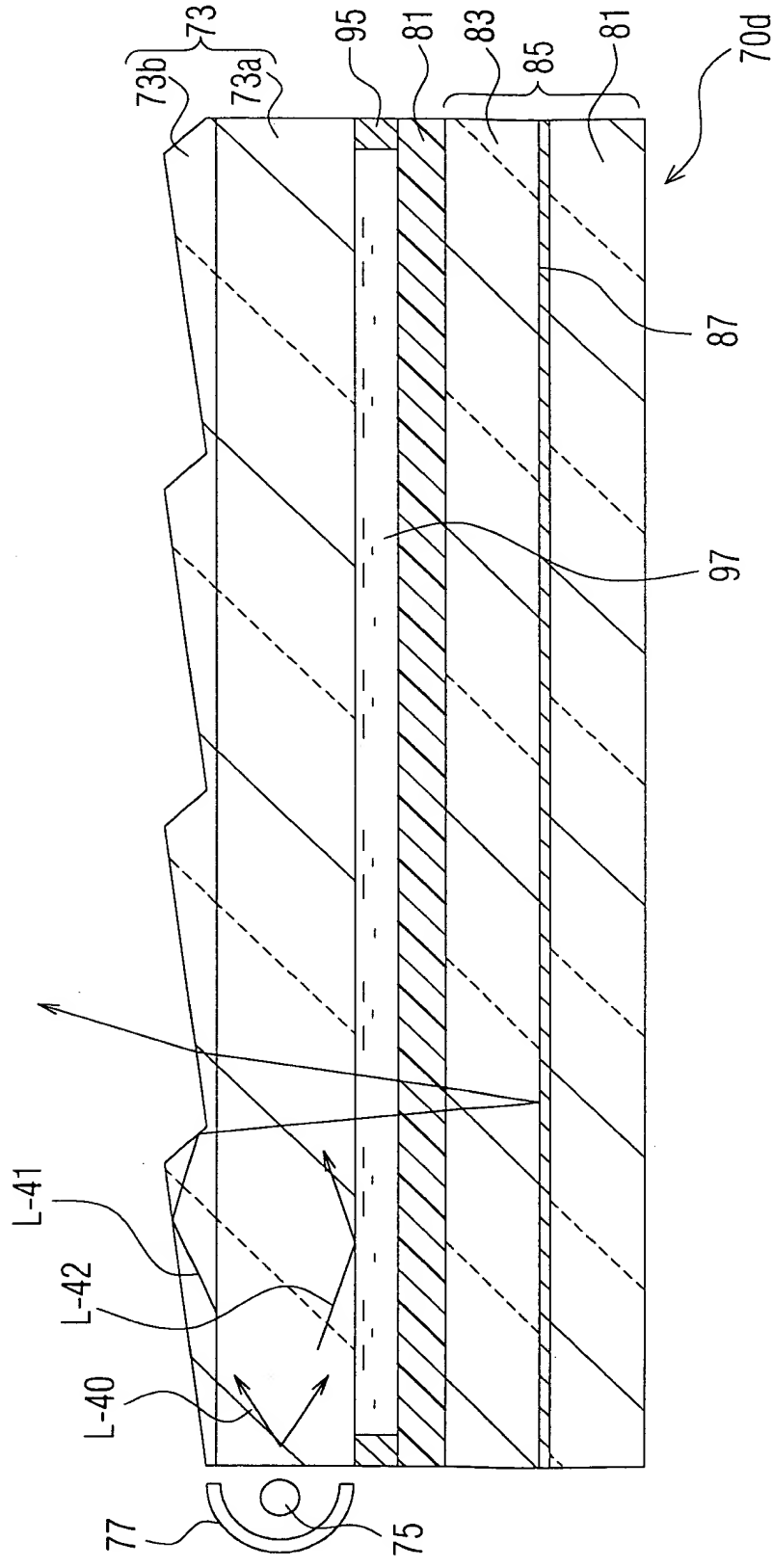




FIG. 16

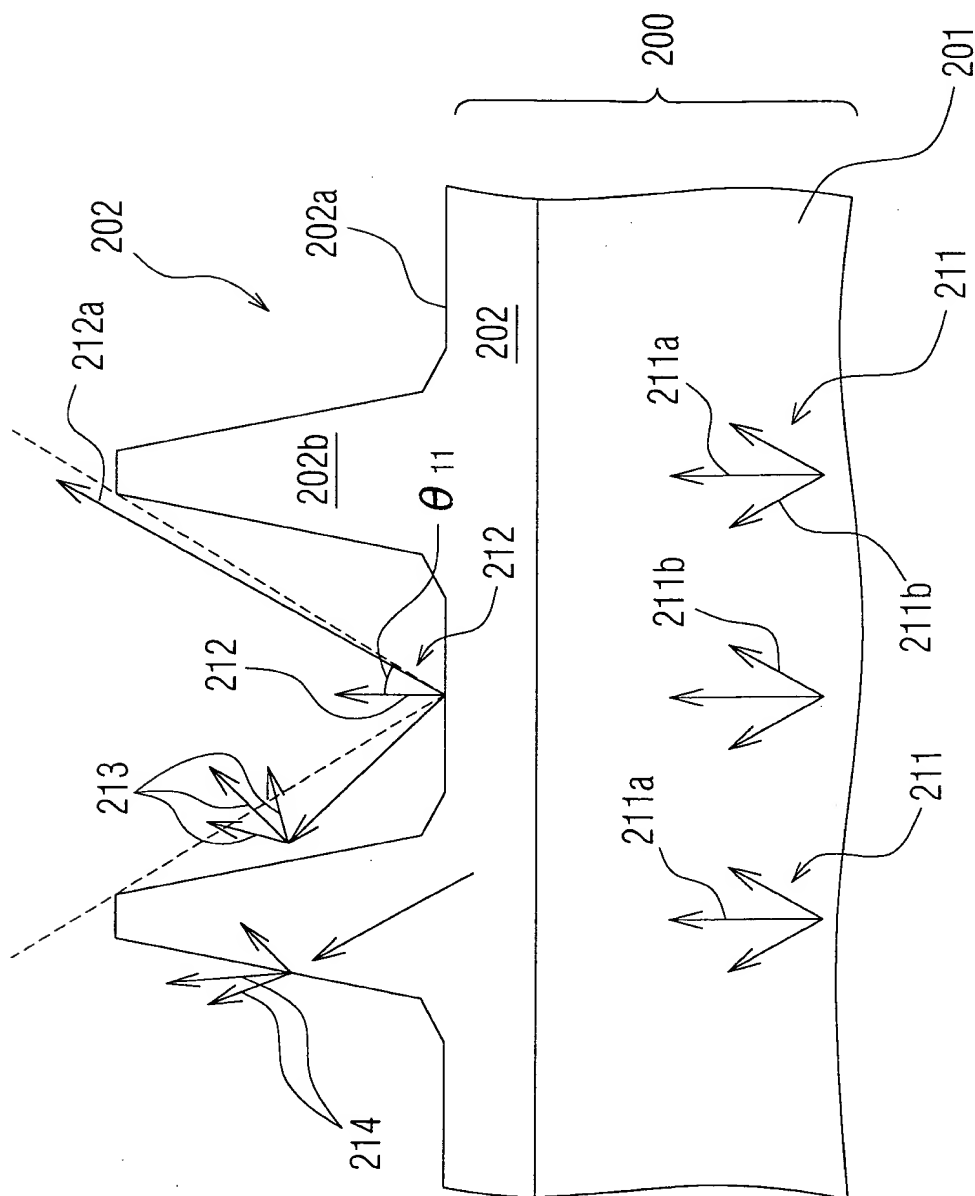


FIG. 17

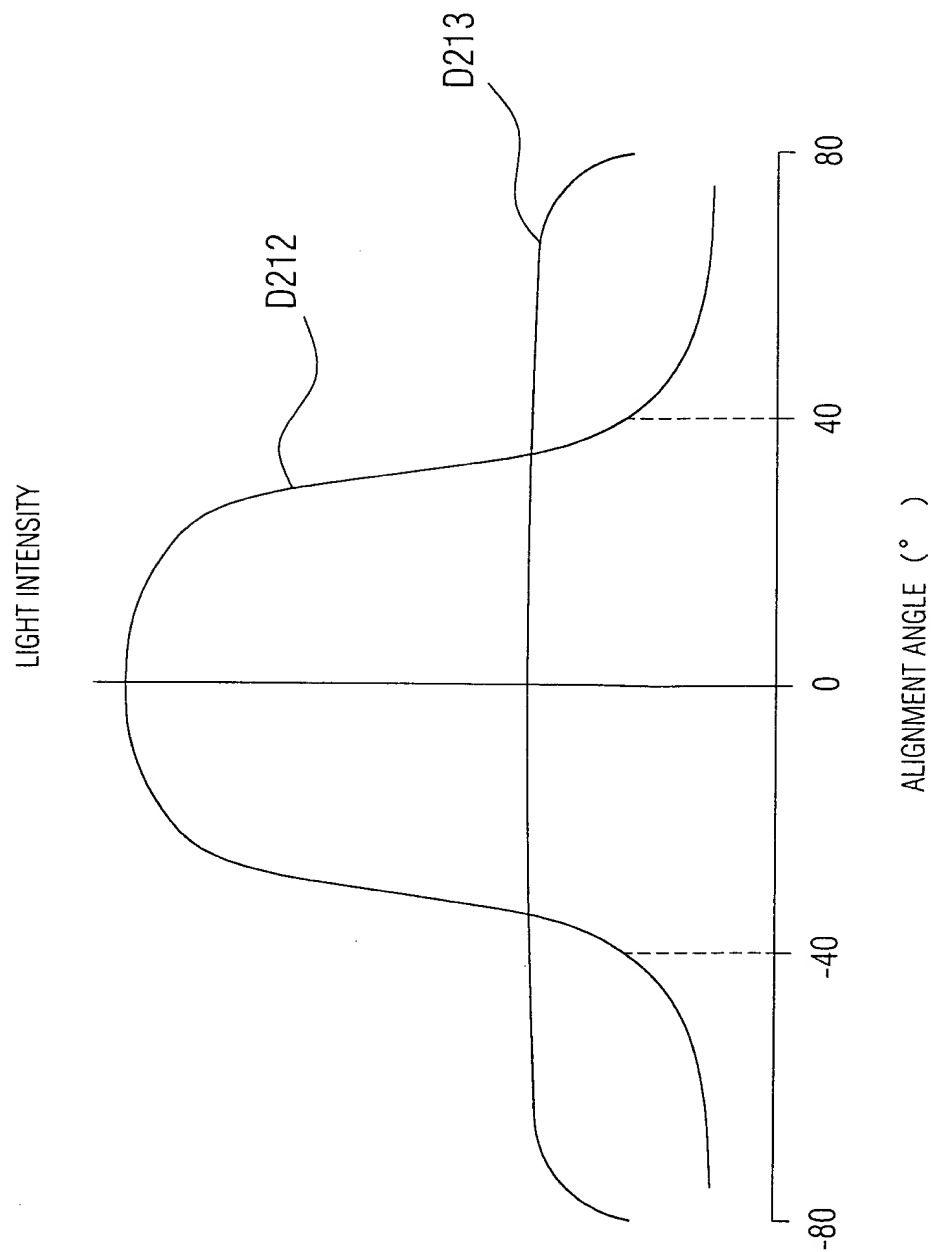
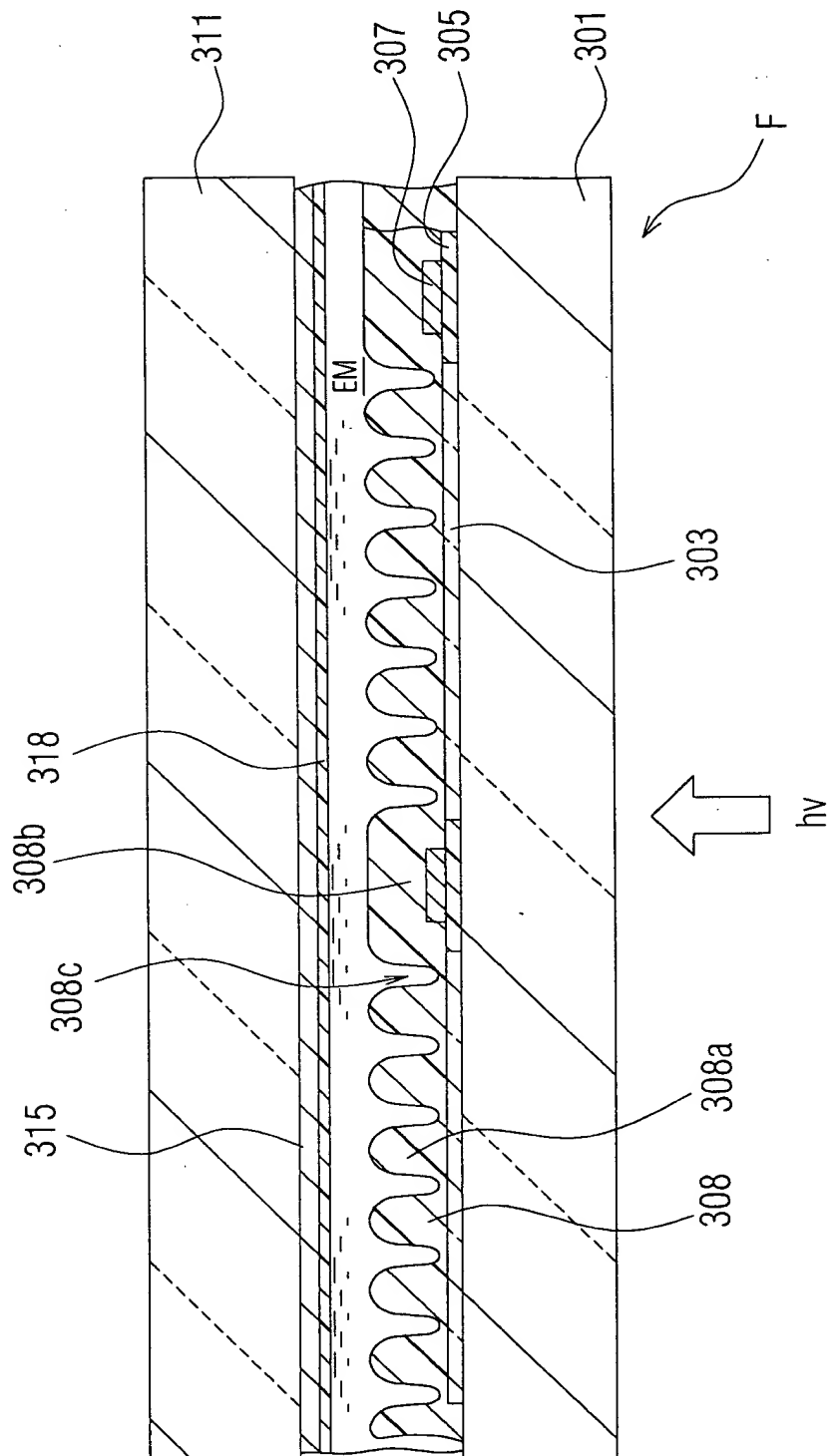


FIG. 18



EM

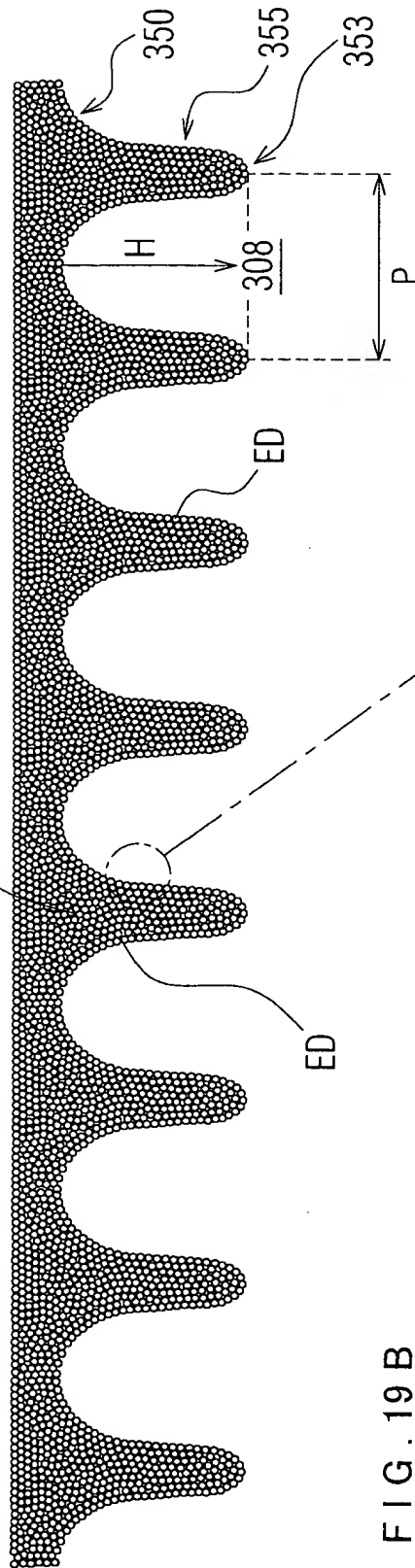


FIG. 19B

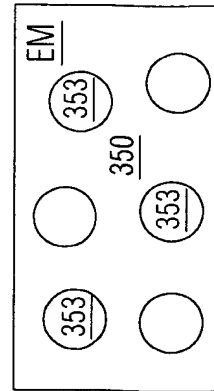


FIG. 19C

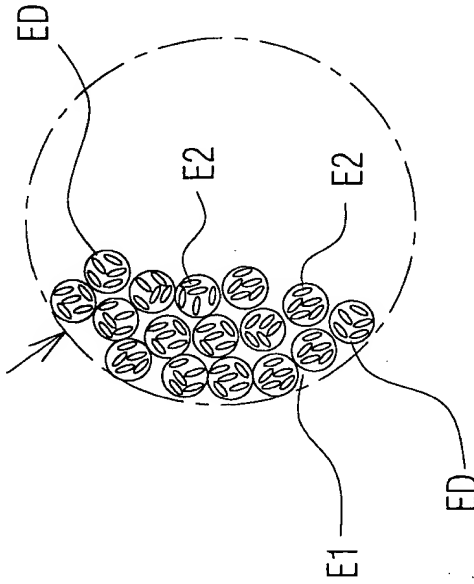
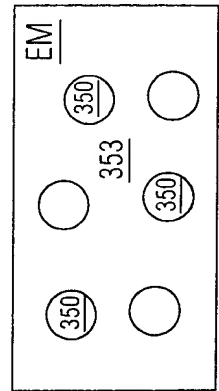




FIG. 21

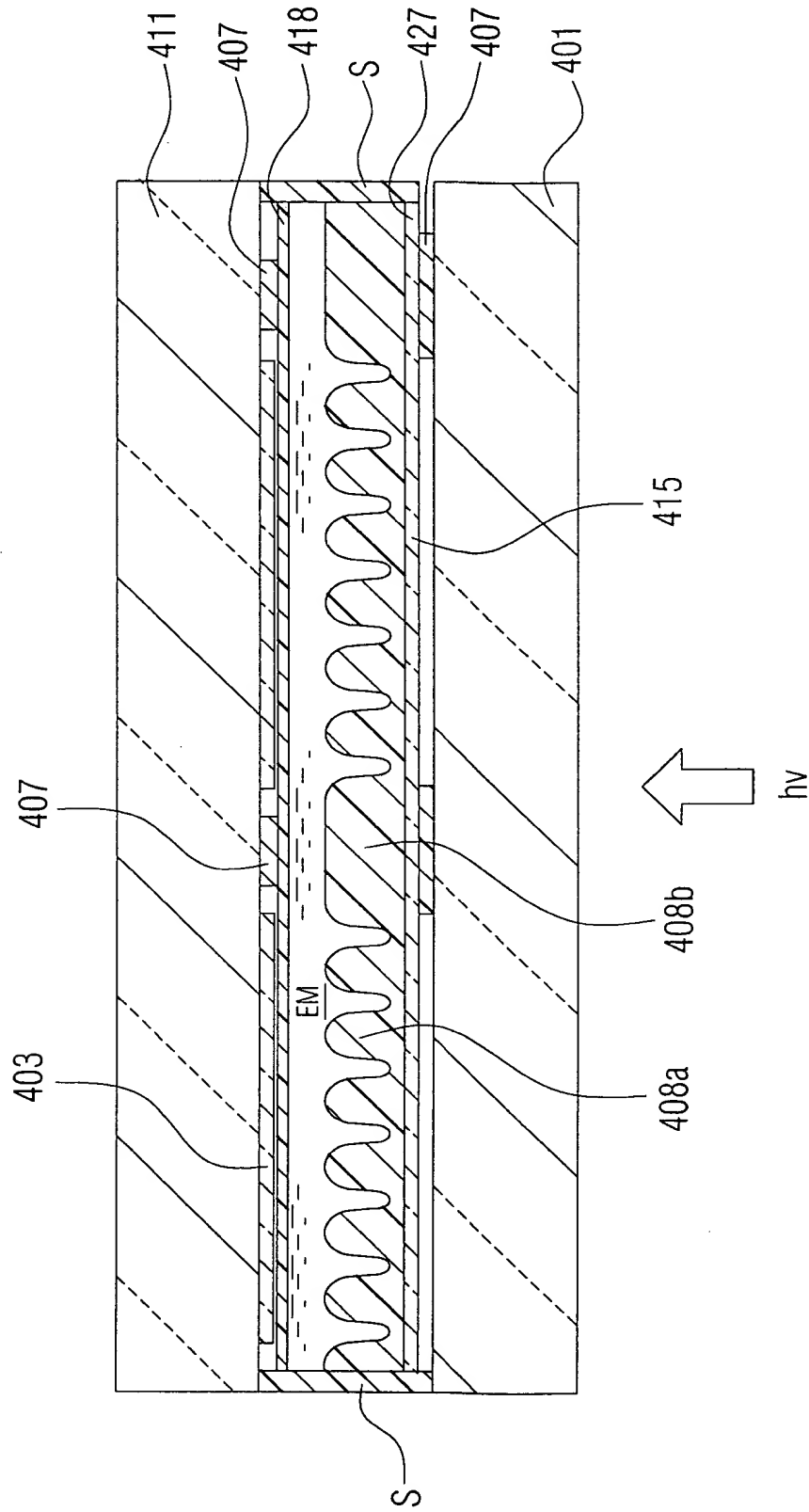


FIG. 22

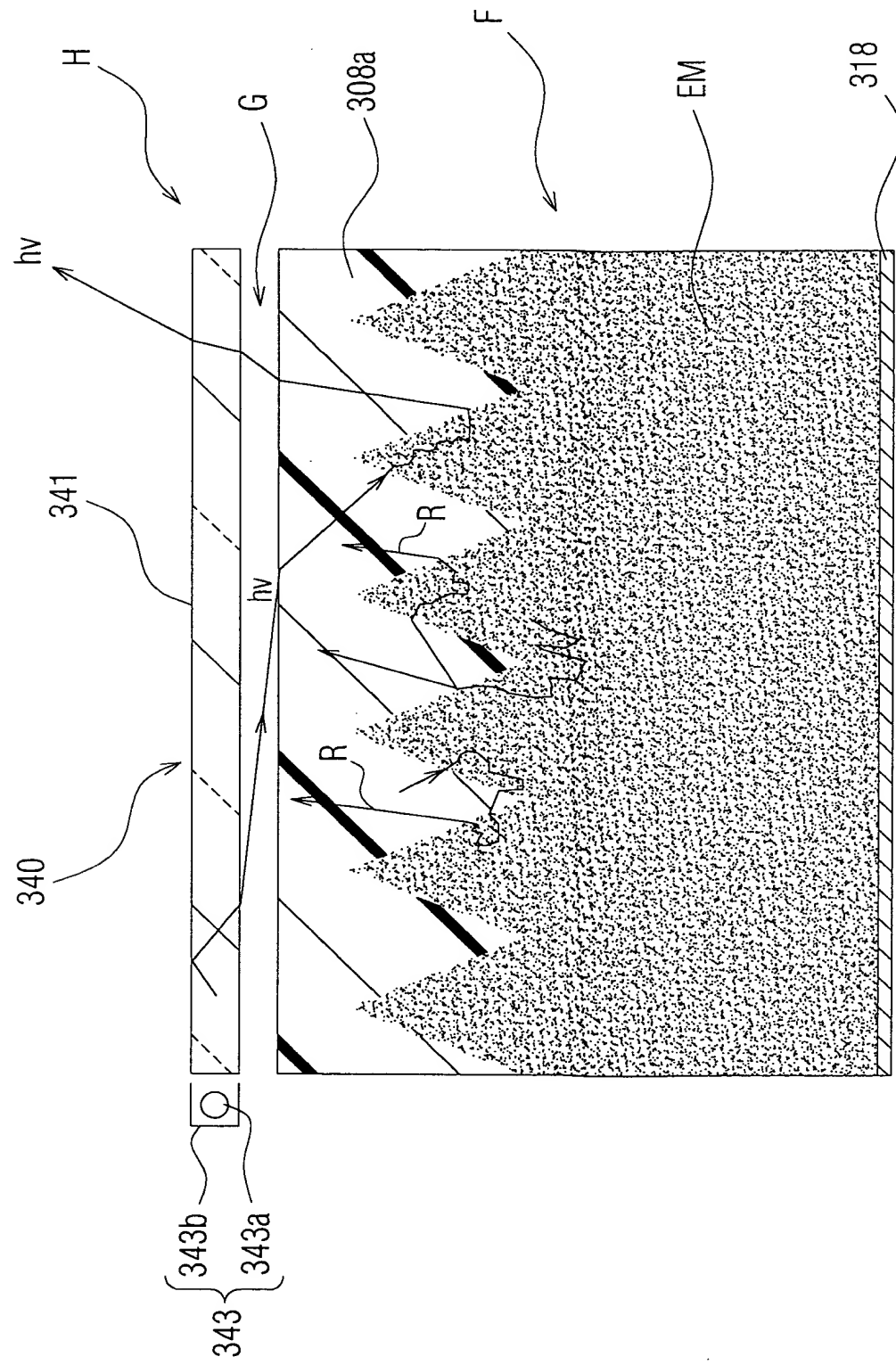


FIG. 23 A

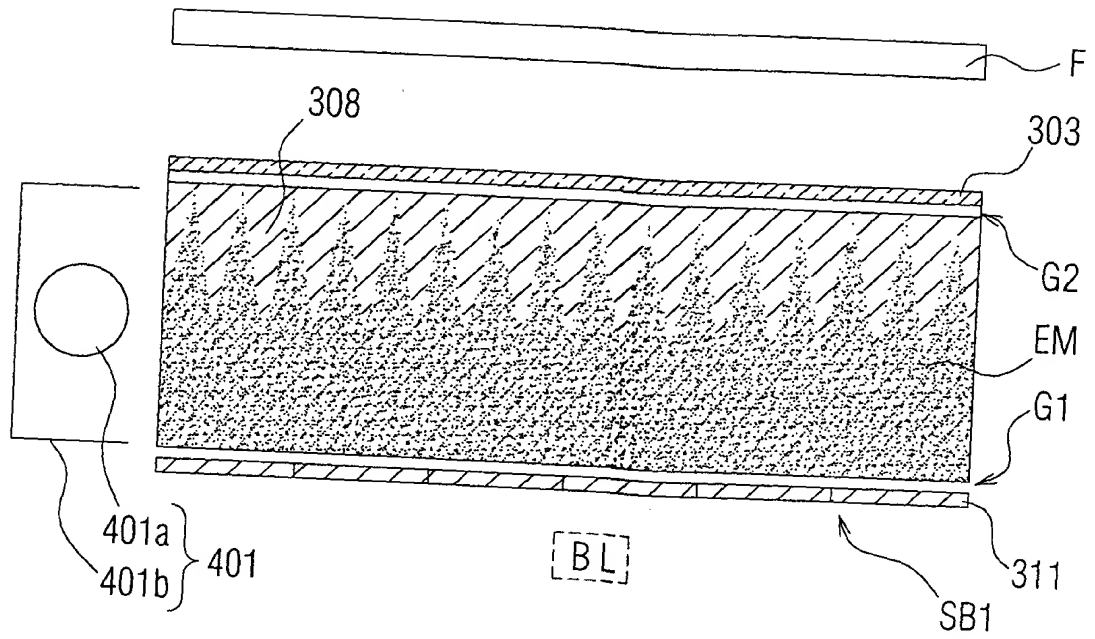


FIG. 23 B

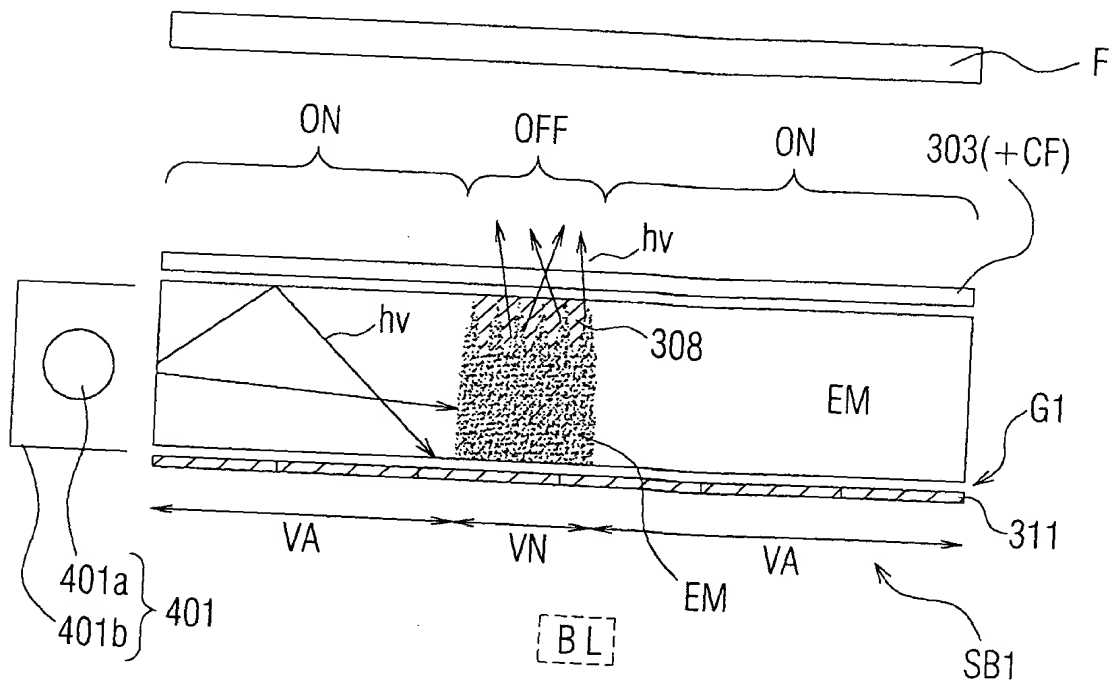




FIG. 24

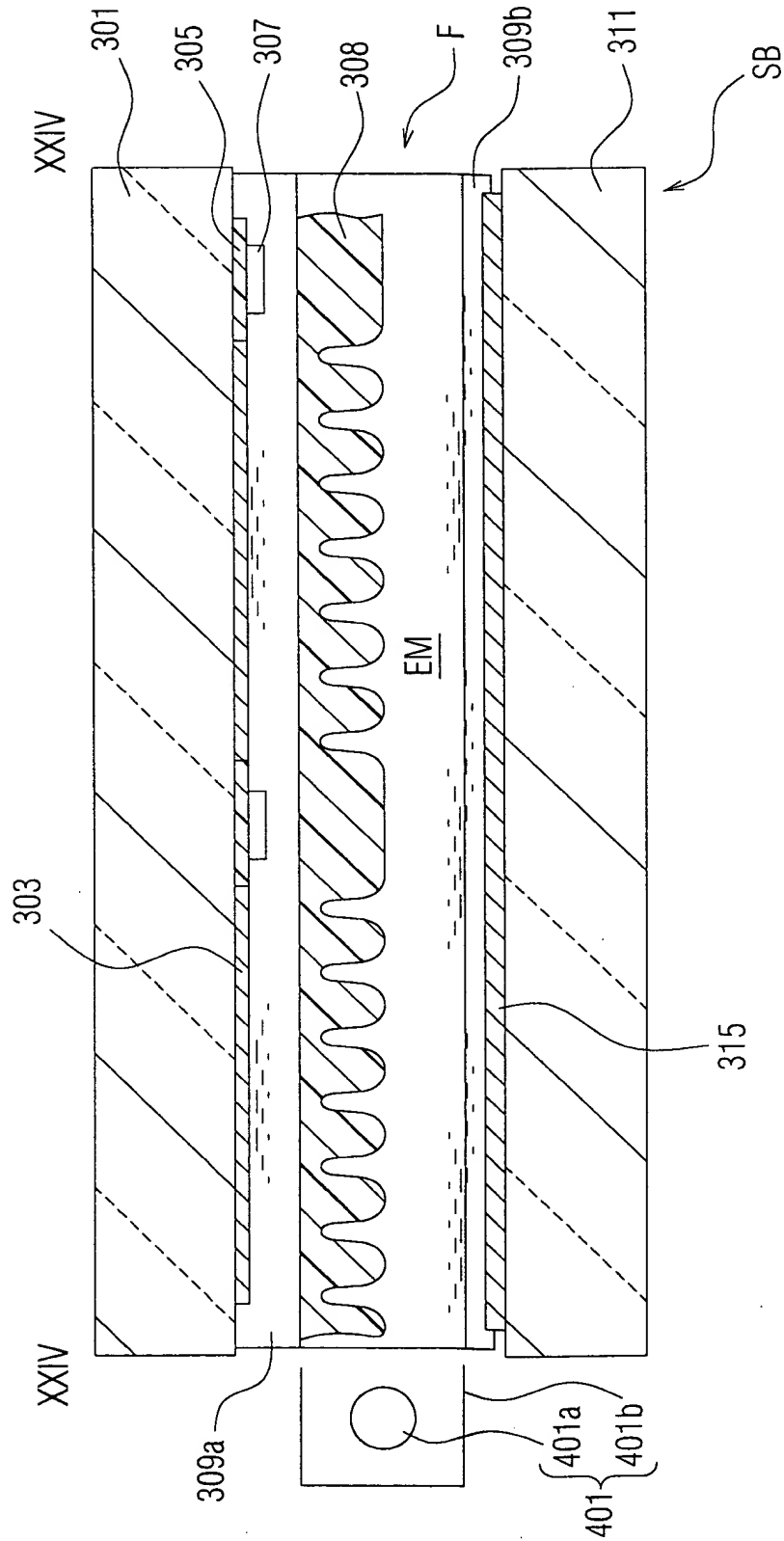


FIG. 25

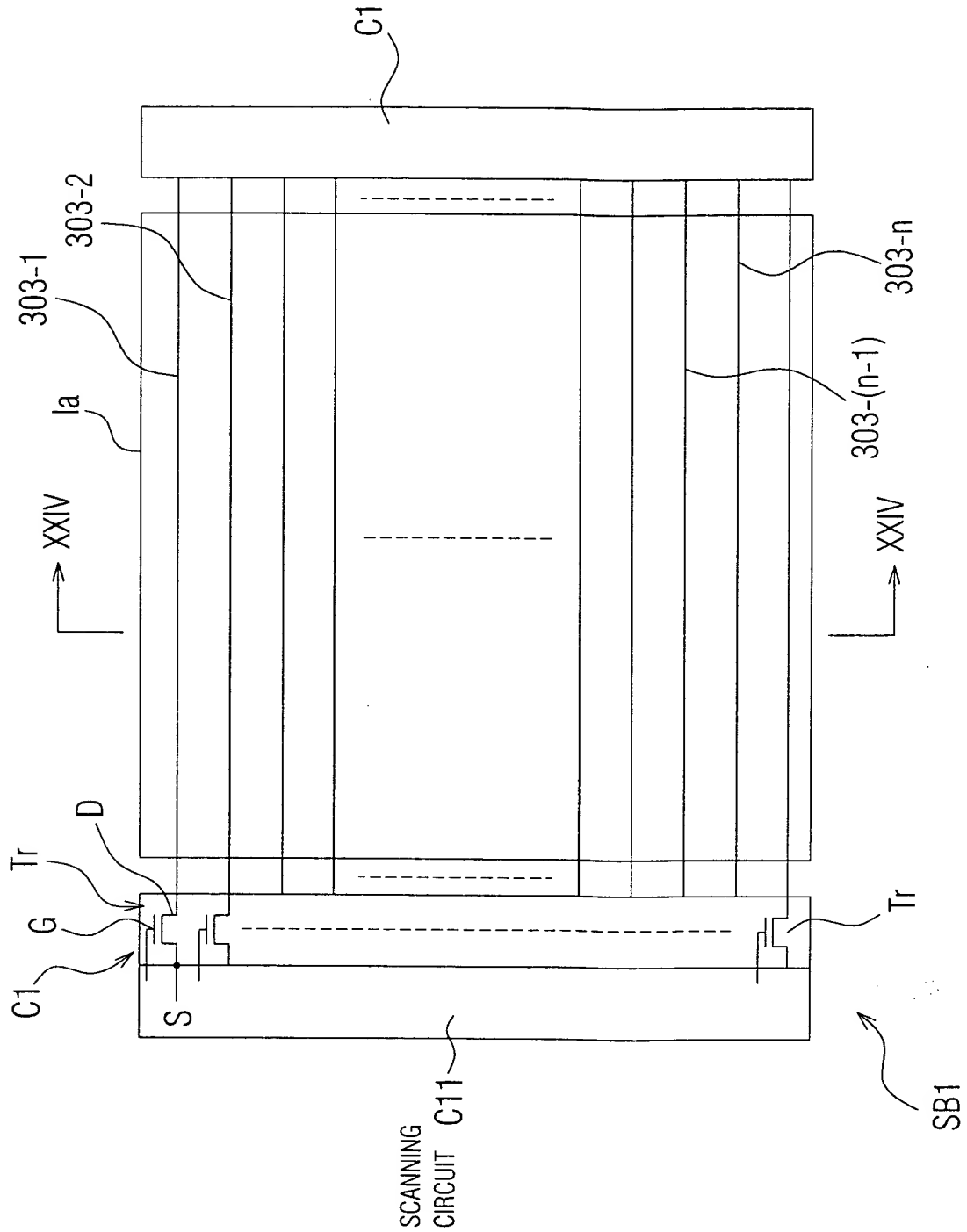




FIG. 27

